REMARKS

Claims 18, 19, 22 and 23 are amended herein. Claims 1-8 and 10-23 remain pending in the application.

35 USC 112 First Paragraph Rejection of Claims 1-8, 10-16, 20 and 21

The Office Action rejected claims 1-8, 10-16, 20 and 21 as allegedly as containing subject matter which is was not described in the specification under 35 USC 112. In particular, the language in claims 1, 7, 13 and 20, i.e., a second agent lacking a dedicated clock, is alleged to lack support in the specification. The Applicants respectfully disagree.

The specification discloses at, e.g., page 9, lines 10-14 that non-super agents receive a clock signal from a super agent. The clock signal may be used as a general processor clock **in place of** an external crystal oscillator.

The Applicants respectfully request the rejection under 35 USC 112 be withdrawn.

35 USC 112 Second Paragraph Rejection of Claims 18 and 19

The Office Action rejected claims 18 and 19 as allegedly being indefinite under 35 USC 112.

The claims have been reviewed and are amended where appropriate. It is respectfully submitted that the claims are now in full conformance with 35 USC 112. It is respectfully requested that the rejection be withdrawn.

Claims 17-19 and 22 over Persaud

In the Office Action, claims 17-19 and 22 were rejected under 35 U.S.C. §102(b) as allegedly being anticipated be Persaud et al., UK Patent Application No. GB2074762 ("Persaud"). Applicants respectfully traverse the rejection.

Claims 17-19 and 22 recite, *inter alia*, accessing a portion of an external non-dedicated shared memory from a second agent based on a

representation of a single memory access clock signal received **from a first agent**.

Persaud appears to teach a system and method for accessing a common memory by a plurality of processors (Persaud, Abstract). A master processor can access its own memory or any of the slave memories (Persaid, Abstract). The master processor generates synchronizing signals which are applied over a backplane to each of the slave processors (Persaud, page 2, lines 45-47). Numerous clocks start to cycle during a POWER ON RESET signal during a reset of a clock generator (Persaud, page 5, lines 48-50). Clock synchronization between the master processor and slave processors is accomplished by sending a REFRESH REQ from the master card to the slave cards (Persaud, page 5, line 60 – page 6, line 16).

Persaud utilizes processors that are driven by a **plurality** of separate dedicated clocks that are normally sychronized, but can become de-synchronized (Persaud, page 2, lines 45-47; page 6, lines 10-11). A synchronization signal from the master processor is used to synchronize the **plurality** of clocks within the slaves. A master processor is synchronized with the slave processor and accesses a slave processor's dedicated memory based on the synchronization of the **plurality** of clocks within the system. Persaud's **plurality** of memory clock signals are received from local clocks, albeit synchronized, **NOT** from a second agent based on a representation of a **single** memory access clock signal received from a first agent, as claimed by claims 17-19 and 22. The Applicants respectfully disagree.

The Office Action alleges Persaud discloses a single memory access clock signal from a first agent (a bus/master continuous 02 signal; claim 19; page 3, lines 15-17; page 5, lines 2-4; first agent is comprised of master processor/clock generator; Fig. 4; references numbers 76, 78 and 126) (Office Action, page 3).

Persaud discloses a synchronization circuit on each slave processor card that operates on the continuous 02 signal generated by the slave oscillator clock to synchronize the **local** 6875 clock generator so that it is in synchronism with the 6875 clock generator on the master card (page 3, lines 14-

19). In this way, all of the processors are synchronized to each other, despite the fact that when power is first turned on, the clock generators may be out of synchronism (Persaud, page 3, lines 19-22).

Persaud discloses a system and method that synchronizes a master clock with slave clocks. Each slave has its own clock generator, i.e., a **local** 6875 circuit, that is synchronized to a master clock signal by a continuous 02 signal. A **plurality** of clock generators is **NOT** a single memory access clock signal, much less a single memory access clock signal that is received **from a first agent**, as claimed by claims 17-19 and 22.

A benefit of having a second agent access a shared memory with a **single** clock signal received from a first agent is, e.g., synchronization through simplicity. Applicants' system requires only a **single** memory access clock, with all agents sharing the signal. A **single** memory access clock signal synchronizing all agents' access to a shared memory possibly eliminates wasted clock cycles during a transfer of access from a first agent to a second agent. In contrast, Persaud requires the use of a dedicated clock generator for each agent. Having a **plurality** of clock generators creates the problem of synchronization (as discussed by Persaud, page 3, lines 1-22).

Accordingly, for at least all the above reasons, claims 17-19 and 22 are patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Claim 23 over Wu

In the Office Action, claim 23 was rejected under 35 U.S.C. §103(a) as allegedly being obvious over Wu et al., Patent No. 5,659,715 ("Wu"). Applicants respectfully traverse the rejection.

Claim 23 recites, *inter alia*, a second agent that lacks a dedicated clock and receives a clock signal representation of a first agent's clock signal for the second agent's access to a non-dedicated shared memory.

Wu appears to teach a first and second processor having access to a common memory bank (Fig. 3, items 302, 400 and 304 respectively). Address and data lines (Wu, items 306 and 308) running to the common memory bank

(Wu, item 304) are routed through a single source, the graphics controller (Wu, item 400). The CPU (item 302) and the graphics controller are tied together to route data to the common memory (Wu, Fig. 3). The common memory is connected to the graphics controller which is connected to the CPU (WU, Fig. 3) Thus, the CPU, the graphics controller and the common memory are synchronized to pass data and address information therebetween with a common clock signal.

Wu teaches utilizing a common clock signal for components accessing a common memory. Components accessing a memory through the use of a common clock signal is **NOT** an agent accessing a memory through a clock signal representation, much less a second agent that lacks a dedicated clock and receives a clock signal representation of a first agent's clock signal for the second agent's access to a non-dedicated shared memory, as claimed by claims 20, 21 and 23.

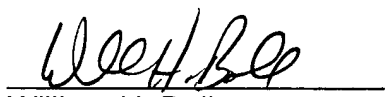
Accordingly, for at least all the above reasons, claim 23 is patentable over the prior art of record. It is therefore respectfully requested that the rejection be withdrawn.

Conclusion

For at least all the above reasons, claims 1-8 and 10-23 are patentable over the prior art of record.

All objections and rejections having been addressed, it is respectfully submitted that the subject application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,



William H. Bollman
Reg. No. 36,457

Manelli Denison & Selter PLLC
2000 M Street, NW
Suite 700
Washington, DC 20036-3307
TEL. (202) 261-1020
FAX. (202) 887-0336

WHB/df